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International Journal of Current Research
Vol. 9, Issue, 10, pp.59766-59771, October, 2017

INTERNATIONAL JOURNAL
OF CURRENT RESEARCH

ISSN: 0975-833X

RESEARCH ARTICLE

DESIGN AND IMPLEMENTATION OF PEER GATE IN 90NM SG TECHNOLOGIES AND QCA

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ARTICLE INFO

Article History:
Received 19th July, 2017
Received in revised form
20th August, 2017
Accepted 29th September, 2017
Published online 31st October, 2017

Key words:
QCA technology,
Peers Gate,
Nano Technology.

ABSTRACT

QCA technology is a promising future nanotechnology for computing. It takes great advantage of a physical effect, the Coulomb force that interacts between electrons. There also exists an alternative implementation that uses magnetic fields, a novel design of a Quantum-dot Cellular Automata (QCA) PeersGate (PG) and its simulation. PeersGate (PG) is a reversible logic gates. Reversible logic gates are attracting a lot of attention due to their zero power dissipation under ideal conditions. Reversible logic circuits are useful for constructing quantum computers. By the adjustment of electrons in a small limited area of only a few square nanometers. QCA is implemented by quadratic cells, the so-called QCA cells. In these squares, exactly four potential wells are located, one in each corner of the QCA cell. In the QCA cells, exactly two electrons are locked in.

Citation: Brahmam, V. and Lakshmi Priya, K. 2017. "Design and implementation of peer gate in 90nm SG technologies and QCA", *International Journal of Current Research*, 9, (10), 59766-59771.

INTRODUCTION

Nowadays the aggressive CMOS devices outputs in several limits like high leakage current, high power density levels, and speed limitations in GHz range. And it is predicated that these limitations eventual end of scaling trend of traditional CMOS technology, the adjustment of electrons in a small limited area of only a few square nanometers. QCA is implemented by quadratic cells, the so-called QCA cells, Quantum – dot Cellular Automata (QCA) is one possible and promising of CMOS technology and it provides a revolutionary approach of computing at Nano-scale. QCA exploits interacting electric or magnetic field polarization. QCA is a novel and potentially attractive Nano-technology due to its extremely small sizes, faster speed, higher scale integration, higher switching frequency, and ultra-low power consumption than transistor based technology.

Explanation of QCA

In contrast to electronics based on transistors, QCA does not operate by the transport of electrons, QCA make use of arrays of coupled quantum dots to encode and process binary information. A four-dot quantum cell consists of four dots positioned at the corners of a square with two extra mobile electrons the QCA Cell consists of four dots at the middle of the sides of cells.

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Electrons can tunnel from dot to dot within a cell, but unable to travel beyond the cell boundaries to neighboring cells, There are two equivalent energetically minimal arrangements for the electrons in a QCA cell i.e. the polarization P = +1 (representing logic 1) and P = –1 (representing logic 0) shown in Fig.1.The QCA cells moves from left-to-right due to electrostatic interactions between adjacent cells. The normal QCA cell is shown in Fig.1 in QCA Inverter Gate is the basic QCA logic element. In this gate signal comes in from the left, splits into two parallel cells, the polarization of the output QCA cell is the opposite of the polarization of input QCA cell. One of the basic QCA fundamental elements is QCA Majority Voter (MV) shown as figure (4), which is a 3-input majority gate and composed of five cells. The remaining cell, labeled OUT (A, B, C), provides the output. This gate performs the Boolean function, OUT(A, B, C) = Maj(A, B, C) = AB+BC+CA. Outputs "1" if there are two or more 1s in an input pattern, otherwise the output is "0".

PeersGate Algorithm and its logic output in 90nm

The Peers gate is implemented in System generator the system generated is block level simulator used for interfacing the Simulink and targeted FPGA. By using system generator we can frame data path from the input of the block to output stage. The clock signals for the SG Can are interpreted by the user so that speed of the overall block can be increased.

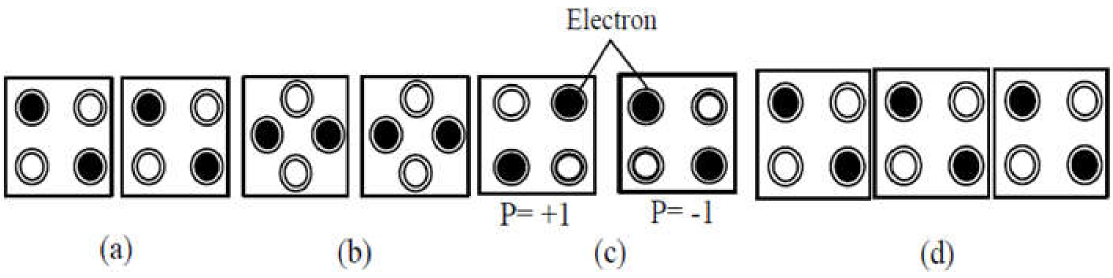


Figure 1.1: (a) QCA Cells with 90- degree orientation (b) QCA Cells with 45-degree orientation (c) Logical representations of QCA Cell (d) Normal QCA wire

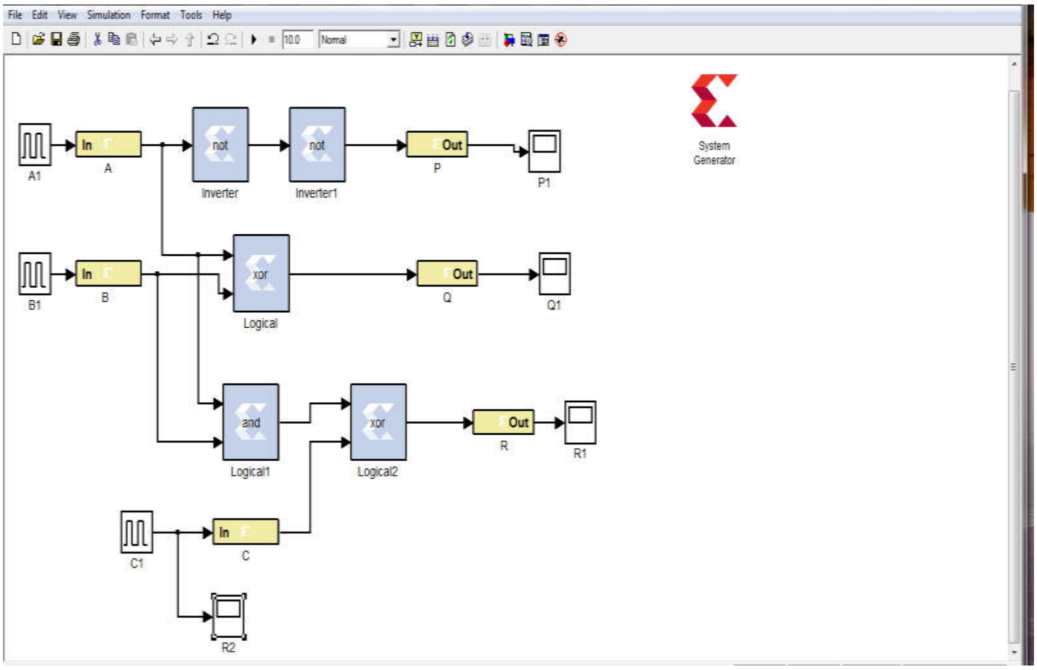


Figure 1.2: System Generator Block Level Simulator

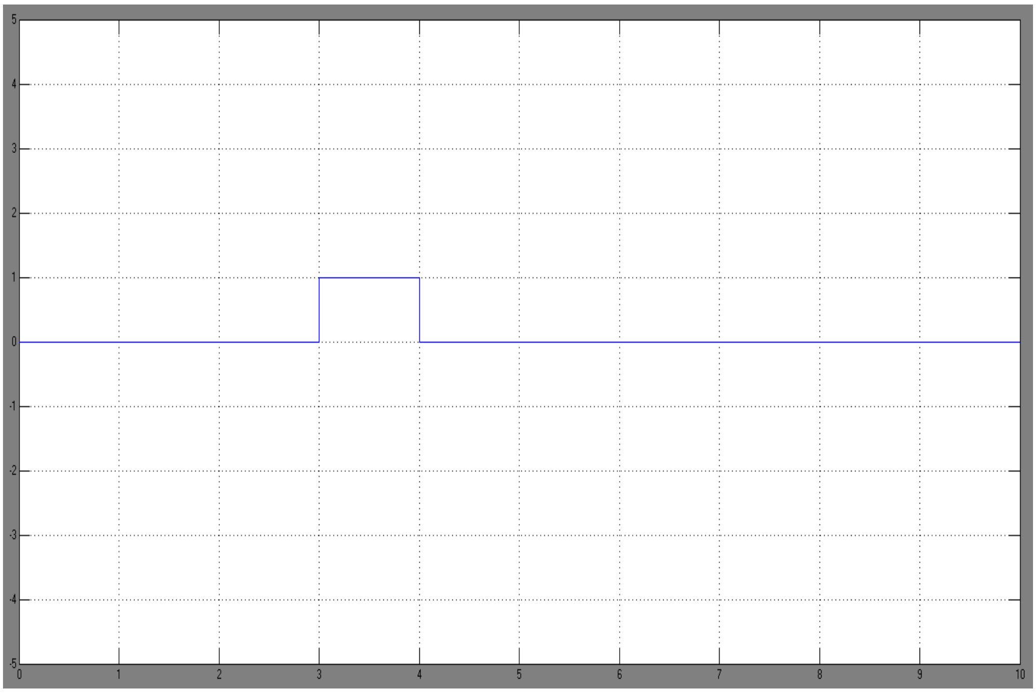


Figure 1.3: Output for P1

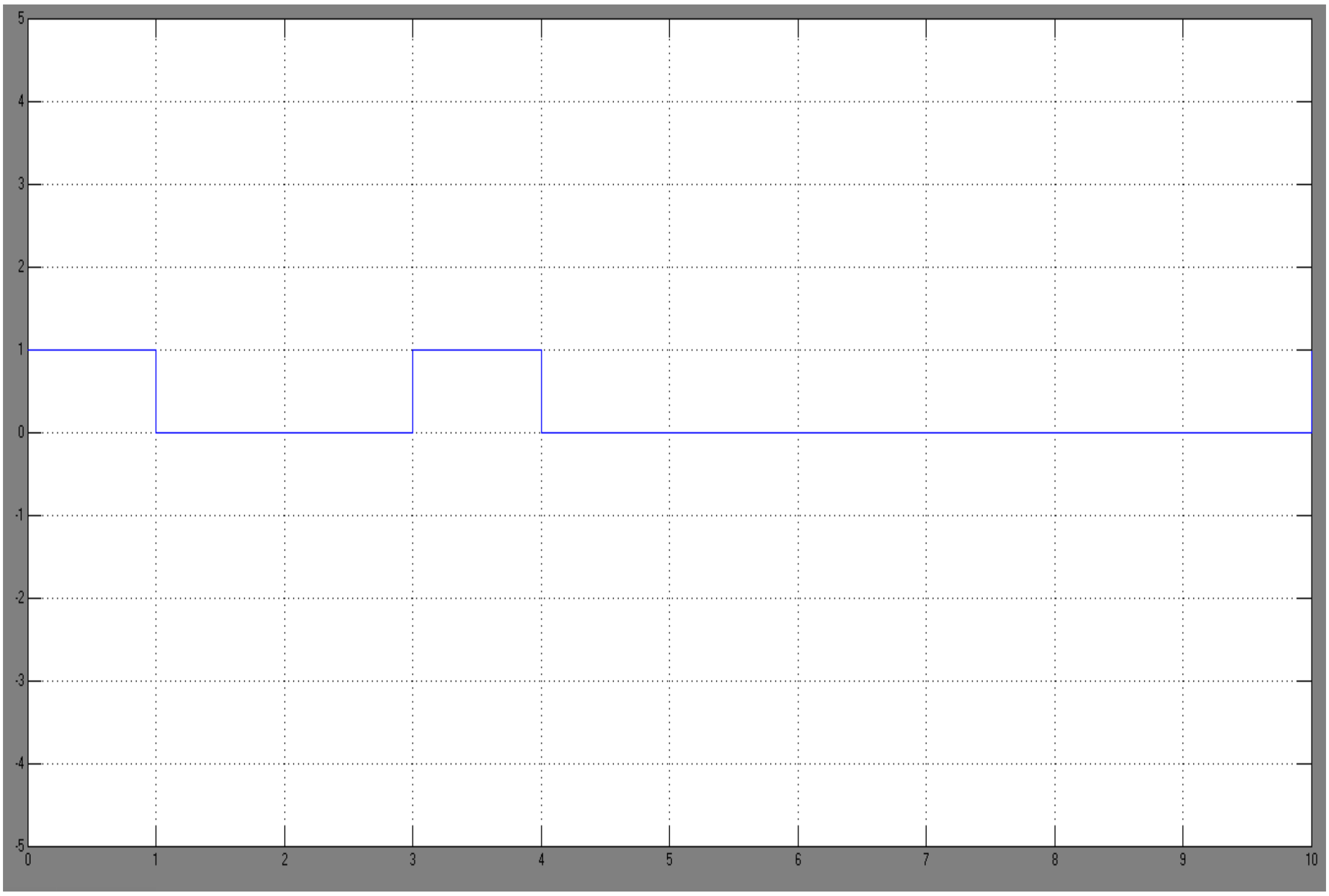


Figure 1.4: Output for Q1

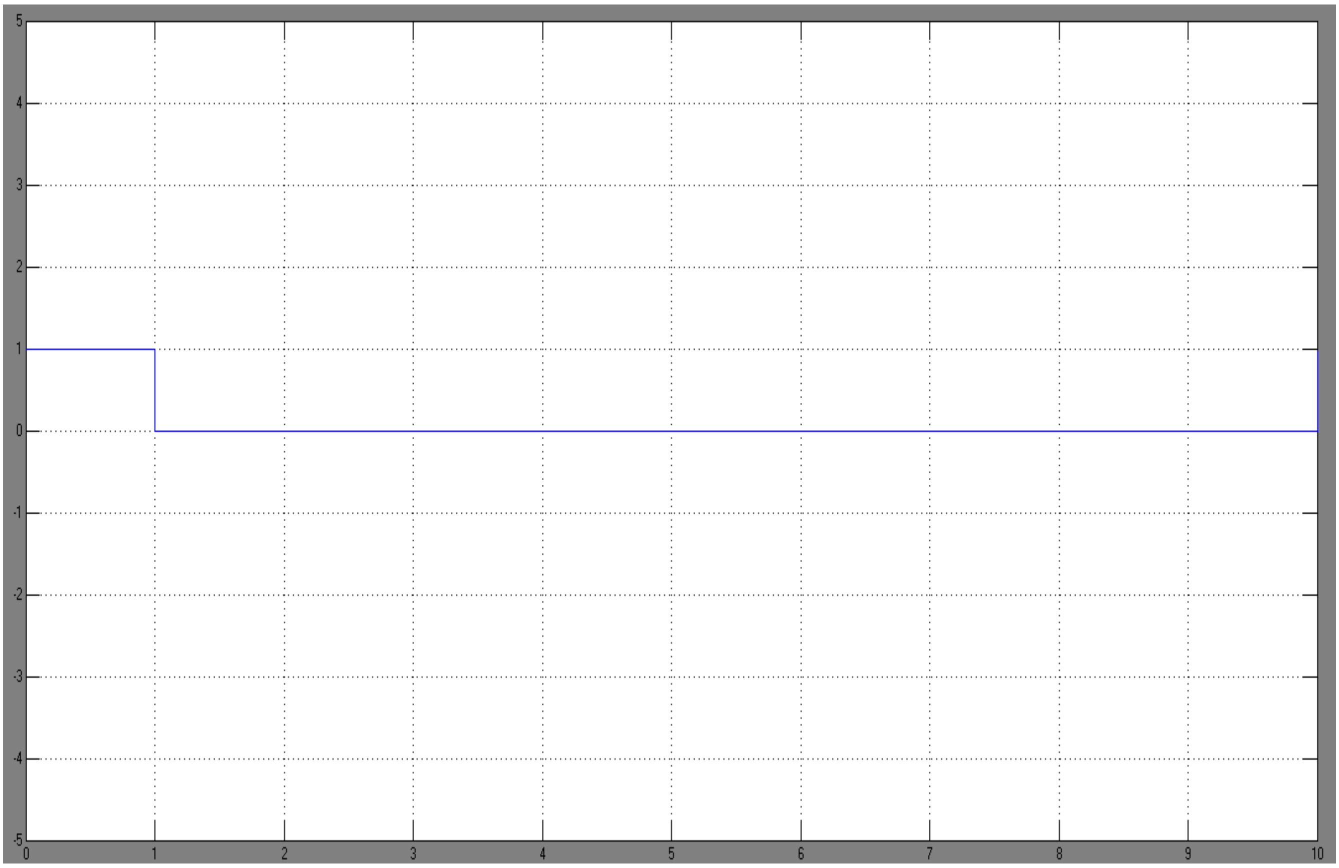


Figure 1.5: Output for R1

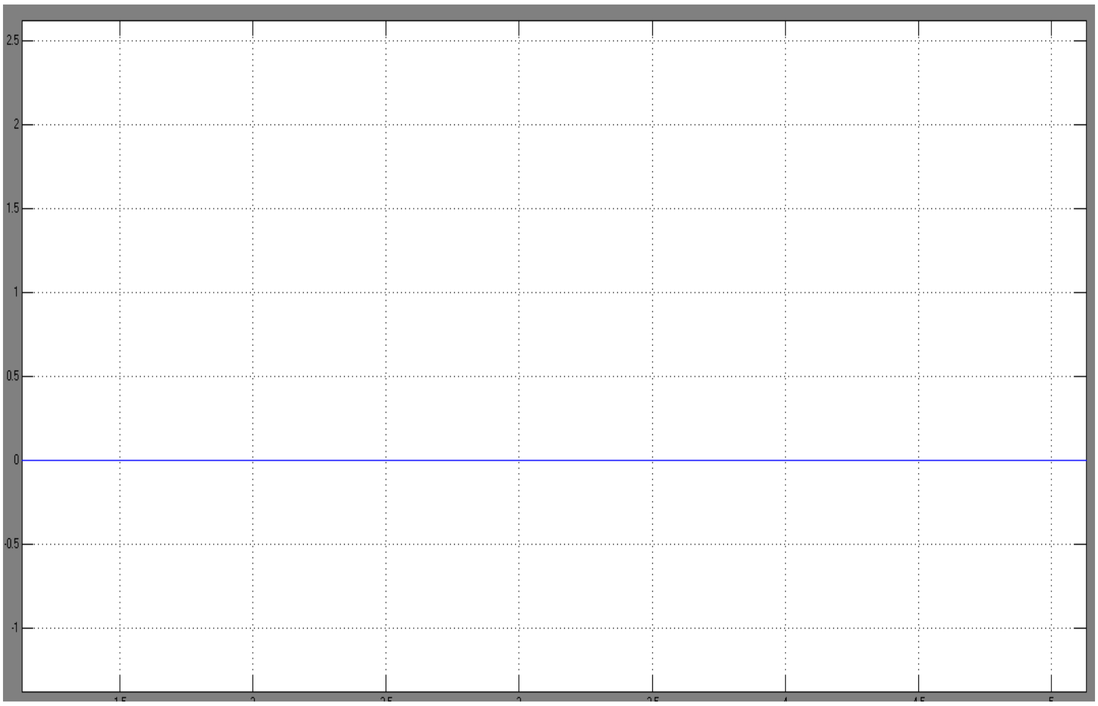


Figure1.6: Output for R2

2.Implementation of XOR Gate

These gates are particularly used in the arithmetic operations and as well as error- detection and correction circuits. XOR and XNOR gates are normally found as 2-input gates. No multiple-input XOR/XNOR gates are available since they are complex to fabricate with hardware. The exclusive-OR (XOR) performs the following logic operation: A⊕B = A'B+ AB'. The QCA implementation for XOR gate is shown in Figure PeersGate (PG) is composed of two XOR gate shown in Figure and one AND gate. Figure shows a 3x3 Peers gate. The input vector is I(A,B,C) and the output vectoris O(P,Q and R). The output is defined by P=A,Q=A⊕B and R=AB⊕C. Quantum cost of a Peers gate is 2.1

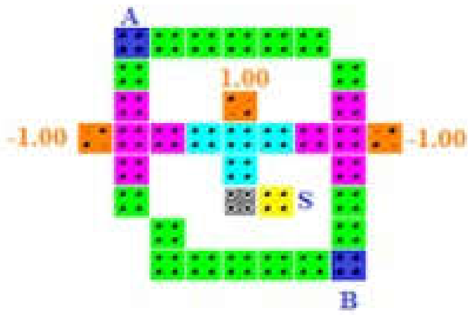


Figure 2.1: Block diagram of XOR Gate

3. PeersGate (PG):

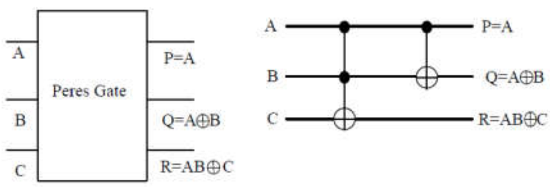


Table 1: Truth Table of Peres Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Figure 4.1: Peers Gate and truth table

3.1. PeersGate (PG) in QCA

The block diagram of PeersGate in QCA is shown in Figure 2.1. The QCA layout structure of the PeersGate is shown in Figure 3.1.1 that is composed of 96 cells. Three of these, representing the inputs to the cell, are labeled A, B and C. Using the terminology of the center cell is the "device cell" that performs the calculation. The remaining cell, labeled P, Q, and R provide outputs. The circuit shown in Figure 3.1.1 performs the Boolean functions P = A, Q = A⊕B and R = AB⊕C.

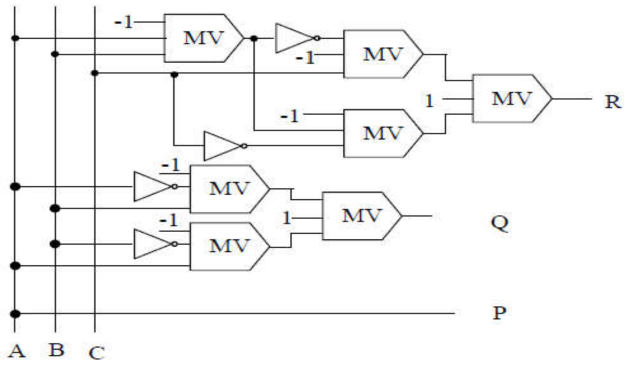
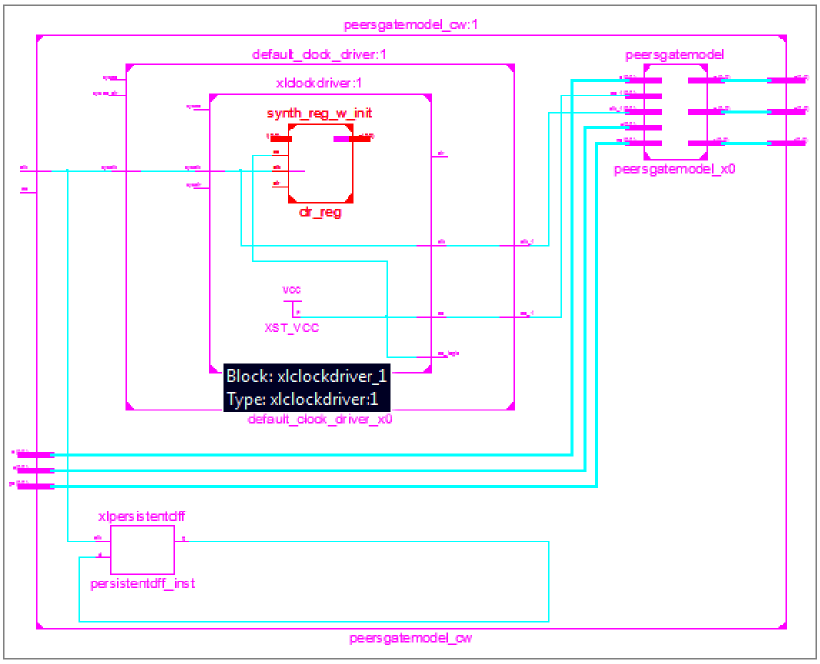


Figure 3.1.1: Peers gate in QCA

4. Peers Gate Model Schematic



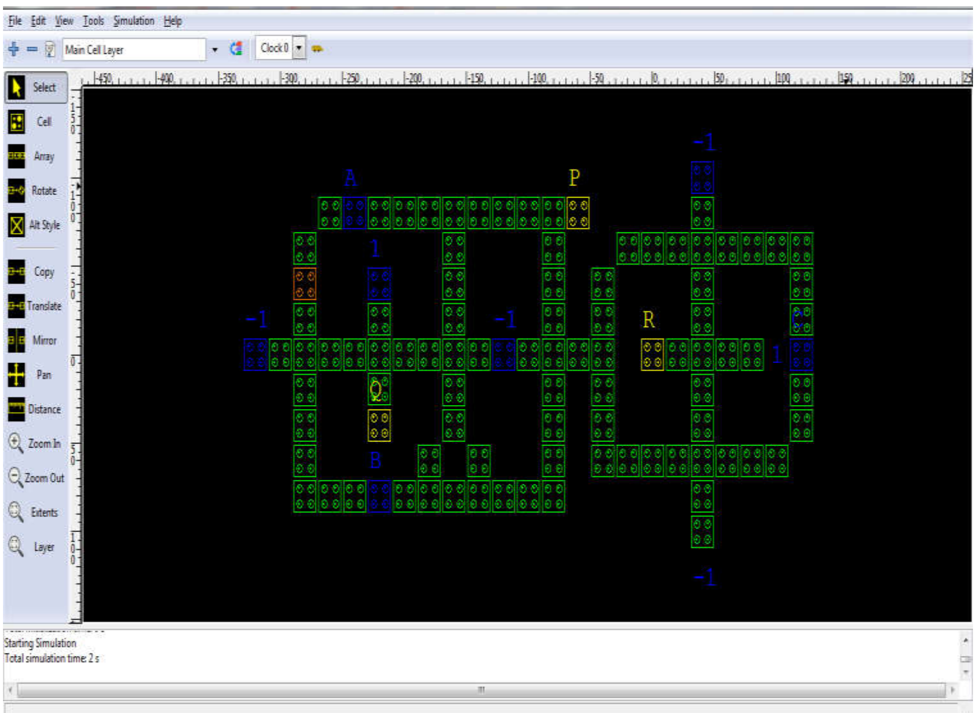


Figure 4.1: Peers Gate Design in System Generator

5. SIMULATION RESULTS

The PeersGate layout has been simulated using QCA Designer version2.0.3; a layout and simulation tool for QCA. The simulation result for a PeersGate is shown in Figure 5.1. In this Simulation we have used the coherence vector computational engine and the following parameters: (18 nm × 18 nm) cell size, 10nm cell-to-cell distances, and 4 nm dot size and 65 nm radius of influence.

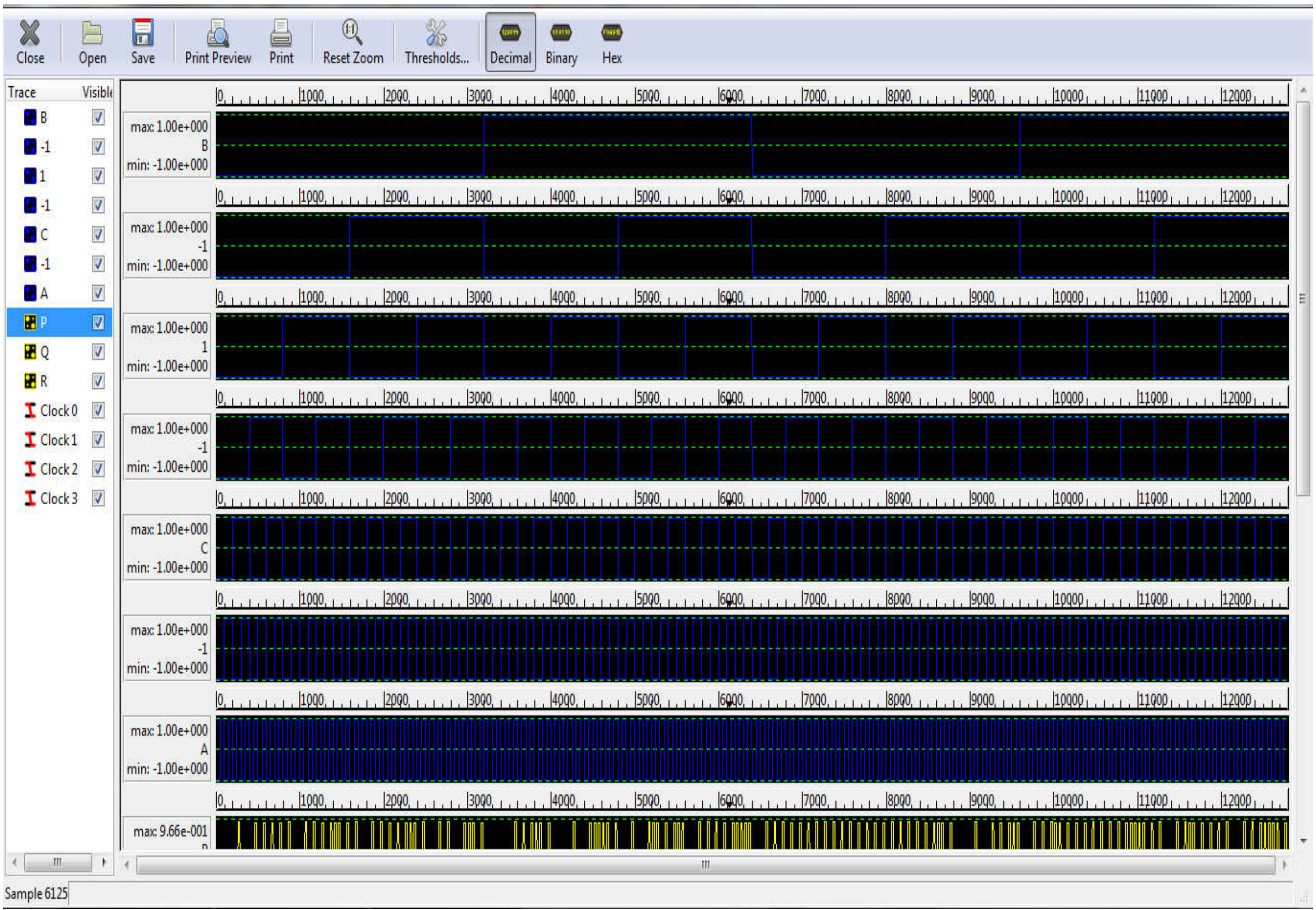


Fig. 5.1. PeersGate Layout

Parameter	Value
Numberofcells	85
Coveredarea(µm2)	0.05
Clockused	4
Timedelay(clockcycle)	1

Table 2. Result proposed Peers Gatein QCA

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