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RESEARCH ARTICLE

FPGA REALIZATION OF RBF NEURAL NETWORK BASED TRANSFORMER IMPULSE FAULT CLASSIFICATION SCHEME

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ABSTRACT

This paper proposes simple hardware architecture for realizing a Radial basis function (RBF) network for transformer impulse fault classification. Fault conditions are applied on the lumped parameter model derived for the DUT and the model is simulated using PSPICE orcad software. The winding currents thus computed are analyzed using db5 wavelet and the statistical features namely mean and Variance are extracted from the third level approximation. The RBF network has a number of advantages compared with other type of ANN including simpler network structure and faster learning speed. The key point of RBFNN is to decide a proper number of hidden nodes. Here the possibilistic FCM algorithm is used to cluster the derived statistical features into 21 different clusters representing the defined fault types and the RBF network is constructed with 21 hidden nodes representing the clusters. The hardware implementation is carried out using Xilinx system generator for DSP on Spartan 6 FPGA. The overall classification accuracy of this scheme is 97%.

INTRODUCTION

Insulation failure within transformers is considered to be one of the most important causes of failure of power transformers. Impulse testing of transformers after assembly is an accepted procedure for the assessment of their winding insulation strength to surge over voltages. It is a routine test as explained standards such as IEC-60076, Part IV, 2002 (IEC 60076 2002). Manufacturing defects or inadequacy of insulation may lead to failure against impulse voltage stresses. Several techniques have been reported in the literature for detecting this fault. A survey of the faults in a transformer as presented in (Bhide *et al.,* 2010) shows that 19% of the total faults occur in the windings and this paper reviews the methods used in practice for detecting winding inter-turn fault. Different from the STFT, the wavelet transform can be used for multi-scale analysis of a signal through dilation and translation, so it can extract time–frequency features of a signal effectively (Rao and Singh 2001). The wavelets have obtained great success in machine fault diagnostics for its many distinct advantages, not only for its ability in the analysis of non-stationary signals. A summary about the application of the wavelet in machine fault diagnostics, including the following main aspects: the time–frequency analysis of signals, the fault feature extraction, the singularity detection for signals, the denoising and extraction of the weak signals, the compression of vibration signals and the system identification has been presented in (Peng and Chu 2004). Studies on the location of power transformer faults during impulse test have been carried out extensively in (Purkait and Chakravorti 2000; Purkait and Chakravorti 2002).

Many fault diagnosis techniques based on fuzzy, neural networks and wavelet transforms have been proposed (Omar and Youssef 2004; Omar and Youssef 2004; Vanamadevi and Santhi 2013; Hung and Wang 2004; Rajamani ?; Attapol Ngaopitakkul and Anantawat Kunakorn 2006; Sendilkumar *et al.,* 2010; Vanamadevi *et al.,* 2008; Ke Meng *et al.,* 2010; Vanamadevi *et al.,* 2014). A method of impulse fault classification had been presented by the authors in which the root mean square value of the fifth level detail signal were extracted and considered for fault classification (Vanamadevi *et al.,* 2008). Another method of impulse fault classification to classify 7 different fault types in which the statistical features extracted from the third level approximation are considered for fault classification by the authors and the classification is achieved with a LVQ Network (Vanamadevi *et al.,* 2014. In the work presented in (Vanamadevi *et al.,* 2014), the authors propose a method for transformer impulse fault classification using RBF network with finer definition of fault types as compared to the work reported previously (Vanamadevi *et al.,* 2014). A novel approach for self-adaptive RBF neural network had been proposed in (Ke Meng *et al.,* 2010) and (Tsung-Yig

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et al., 2009). The work presented in (Tsung-Yig *et al.,* 2009) has proposed the RBF neural network based DGA method for power transformer fault diagnosis.

FPGAs with their concurrent processing capability are suitable for implementation of ANNs. An extensive review of the deployment of FPGA in industrial control systems is covered in (Eric Monmasson and Marcian N. Cirstea 2007). FPGA realization of a fast hardware efficient logic for fault detection and classification in transmission lines had been presented in (Simi P.Valsan and Shanthi Swarup 2009). FPGA based Induction motor failure monitoring embedded system is presented in (Rodriguez-Donate *et al.,* 2009). An efficient impulse fault classification scheme consisting of parallel LVQ neural network for impulse fault classificationand DWT based feature extraction had been implemented on FPGA by the author in (Vanamadevi *et al.,* 2014). The focus of this paper is to propose simple hardware architecture for realizing a trained Radial basis function (RBF) network on an FPGA. In this work, the authors propose a method for transformer impulse fault classification of 21 different fault types. To achieve good impulse fault classification the PFCM clustering algorithm (Neelam Kumari *et al.,* 2012) is used in this scheme to group the statistical features extracted from the winding currents under 79 different fault conditions into 21 distinct clusters. The Radial basis function network is constructed with a hidden layer of 21 nodes whose Gaussian functions have their center parameters made equal to the cluster centers of these 21 clusters and width parameter equal to 1. The FPGA realization of the proposed scheme is carried out in the MATLAB simulink environment with Xilinx system generator for DSP. The proposed scheme is able to classify the defined transformer impulse faults with 97% classification efficiency.

Feature extraction for impulse fault classification

A. Simulation of the Lumped Parameter model

A specially designed 6.6kv voltage transformer winding is considered as the device under test (DUT). The simulation work is carried out with the ten section lumped parameter model derived for the DUT through measurement and calculation using formulae (Grover Fredrick 1946) based on the geometry of the winding. The lumped parameter model is excited with a signal defined similar to a standard lightning impulse (LI) of 1V amplitude, 1.2/50µs as front time and fall time respectively. The winding current through a current viewing resistor R as shown in Figure 1 is recorded under no fault and different simulated fault conditions. The ten sections of the lumped parameter model is divided into three regions namely line end (sections 1 up to 3), mid-winding (sections 4 up to 7) and neutral end (sections 8 up to 10). The objective is to determine a detection and classification strategy by considering the presence of only series faults or only shunt faults in the three regions, or the simultaneous presence of shunt fault in sections of one region and series fault in any of the sections of the other two regions of the winding.

The circuit simulation of the model is carried out to obtain 79 winding current data set corresponding to the no fault and various simulated fault conditions (Vanamadevi *et al.,* 2014).

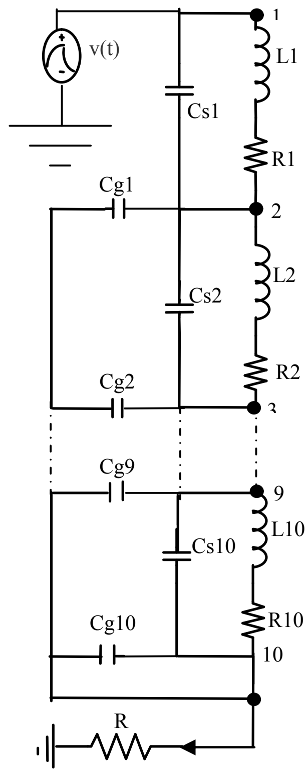

Fig. 1. Lumped parameter model of the DUT

The series faults are simulated by placing a short across a section and shunt faults are simulated by placing a short across a section end and ground. The winding currents are recorded at a sampling frequency of 10MHz. The record length of the winding current is 1mS, and the total number of data points is 10028. A sample of winding currents recorded under simultaneous presence of shunt and series faults are shown in Fig. 2, Fig. 3 and Fig. 4.

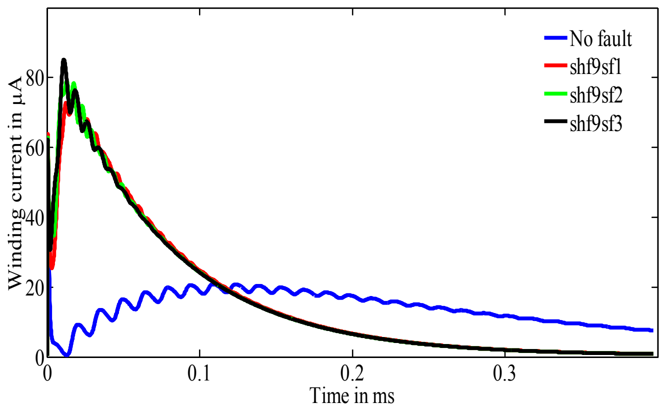

Fig. 2. Winding currents due to shunt fault in section 9 (neutral-end) and series fault in the line end sections

Extraction of statistical Discrimination features

In this work third level approximation is analyzed to extract the features in view of the fact that this level frequency band includes the resonant peaks of the DUT.

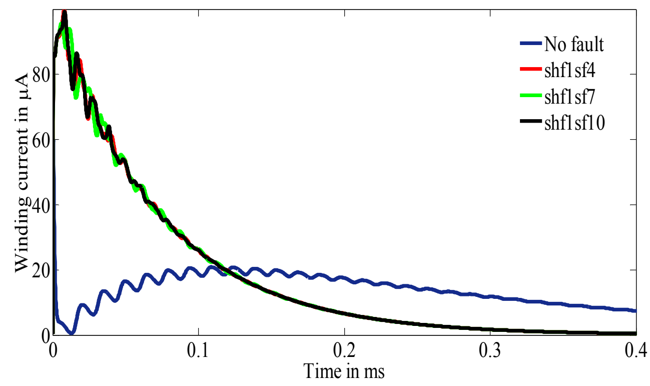

Fig. 3. Winding currents due to shunt fault in section 1(line-end) and series fault in mid-winding/neutral-end sections

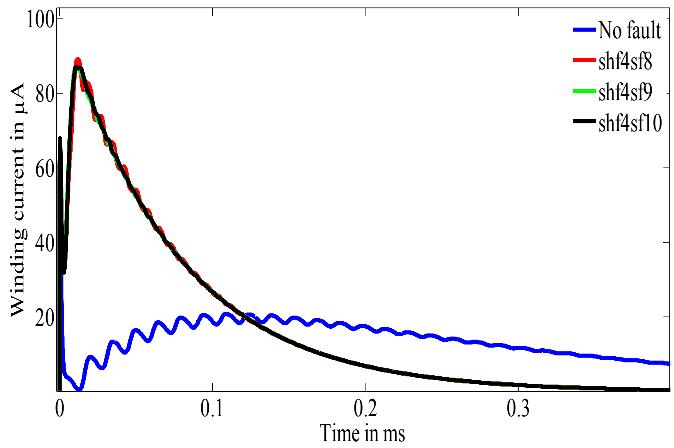

Fig. 4. Winding currents due to shunt fault in section 4(mid-winding) and series fault in neutral-end sections.

An approximation contains the general trend of the original signal. The dB5 wavelet is chosen here as the mother wavelet as this wavelet is most widely used for fault detection applications. The statistical analysis of the third level approximation of the no fault winding current and winding currents recorded under series, shunt and simultaneous presence of series and shunt fault conditions are carried out using the designed DWT analysis filter bank followed by mean-variance computation block given in Fig.5 (Vanamadevi *et al.,* 2014). The statistical features extracted are tabulated in Table 1 and Table 2.

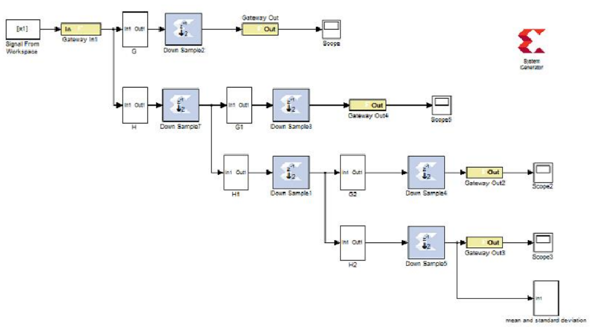

Fig. 5. Simulink model of DWT analysis filter bank and mean-variance computation logic using Xilinx system generator for DSP

Table 1. Statistical feature under presence of only series/ only shunt faults

Fault type	Mean	Std.dev.
nf	1.99E-05	3.57E-10
sf1	1.90E-05	1.14E-09
sf2	1.90E-05	1.21E-09
sf3	1.90E-05	1.28E-09
sf4	1.90E-05	1.33E-09
sf5	1.90E-05	1.35E-09
sf6	1.90E-05	1.35E-09
sf7	1.90E-05	1.36E-09
sf8	1.90E-05	1.32E-09
sf9	1.90E-05	1.27E-09
sf10	1.91E-05	1.22E-09
shf1	2.09E-05	2.52E-09
shf2	2.08E-05	2.46E-09
shf3	2.07E-05	2.38E-09
shf4	2.05E-05	2.28E-09
shf5	2.03E-05	2.16E-09
shf6	2.01E-05	2.01E-09
shf7	1.98E-05	1.84E-09
shf8	1.95E-05	1.61E-09
shf9	1.91E-05	1.22E-09

Table 2. Statistical features under simultaneous presence of series and shunt faults

Fault type	Mean	Std.dev.
shf1sf(4-10)	2.088E-05	2.523E-09
shf2sf(4-10)	2.077E-05	2.463E-09
shf3sf(4-10)	2.064E-05	2.375E-09
shf4sf1	2.065E-05	2.417E-09
shf4sf2	2.065E-05	2.414E-09
shf4sf3	2.064E-05	2.397E-09
shf5sf1	2.050E-05	2.272E-09
shf5sf2	2.052E-05	2.271E-09
shf5sf3	2.052E-05	2.277E-09
shf6sf1	2.049E-05	2.338E-09
shf6sf2	2.051E-05	2.342E-09
shf6sf3	2.050E-05	2.324E-09
shf7sf1	2.034E-05	2.154E-09
shf7sf2	2.034E-05	2.142E-09
shf7sf3	2.034E-05	2.150E-09
shf4sf8	2.031E-05	2.248E-09
shf4sf9	2.031E-05	2.253E-09
shf4sf10	2.033E-05	2.245E-09
shf5sf8	2.012E-05	2.009E-09
shf5sf9	2.012E-05	2.003E-09
shf5sf10	2.012E-05	2.000E-09
shf6sf8	2.007E-05	2.144E-09
shf6sf9	2.008E-05	2.152E-09
shf6sf10	2.008E-05	2.144E-09
shf7sf8	1.984E-05	1.825E-09
shf7sf9	1.984E-05	1.836E-09
shf7sf10	1.984E-05	1.828E-09
shf8sf1	1.975E-05	2.001E-09
shf8sf2	1.976E-05	2.026E-09
shf8sf3	1.977E-05	2.019E-09
shf9sf1	1.978E-05	2.012E-09
shf9sf2	1.979E-05	1.988E-09
shf9sf3	1.980E-05	1.936E-09
shf8sf4	1.982E-05	1.872E-09
shf8sf5	1.933E-05	1.773E-09
shf8sf6	1.934E-05	1.816E-09
shf8sf7	1.934E-05	1.827E-09
shf9sf4	1.935E-05	1.835E-09
shf9sf5	1.937E-05	1.820E-09
shf9sf6	1.938E-05	1.787E-09
shf9sf7	1.941E-05	1.720E-09

These features have promising level of discrimination among the 21 different fault types and is obvious from Fig.6 which show that the features belonging to different fault types almost fall in separate clusters.

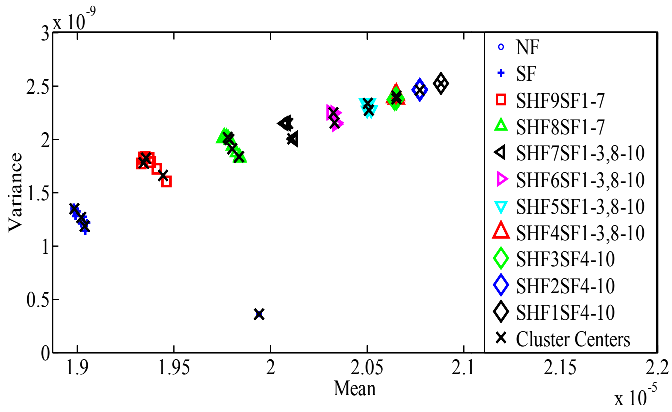

Fig.6. Statistical features extracted from the winding currents due to no fault and different fault conditions

Design of Radial Basis Function Neural Network for Impulse fault Classification

A Radial basis function network is a pattern classifier net having a feed forward network. Classification task is performed by transforming the pattern into a high dimensional space in a non-linear manner. It requires less training time than the other multilayer neural network to achieve the same performance. The construction of a Radial Basis Function neural Network, in its most basic form given in Fig.7 involves three layers with entirely different roles. The input layer is made up of source nodes (sensory units) that connect the network to its environment. The second layer, the only hidden layer in this network, applies a non linear transformation from the input space to the hidden space. In most applications the hidden space is of high dimensionality. Each node in the hidden layer finds out the radial distance from center to each point on the associated radial basis function. The output layer is linear and provides the response of the network to the activation pattern applied to the input layer.

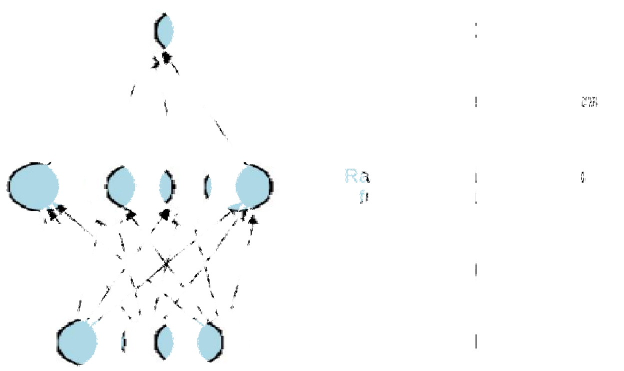

Fig. 7. Radial basis function network designed for impulse fault classification

The statistical features extracted are grouped into 21 distinct clusters using PFCM algorithm (Neelam Kumari *et al.*, 2012). These are the possible distinct clusters that could be obtained with 79 dataset representing various fault conditions. Hence Radial basis function neural network is constructed with 21 hidden nodes. The Gaussian function's center parameters of the hidden layer nodes are assigned with the determined cluster center values and the width parameter values are assigned unity. Out of the 79 dataset, the RBF network is trained with 43 dataset falling under 21 defined fault types and tested with remaining data. Table 3 lists the defined fault types and their respective fault number which are considered as the target while training the network. The RBF network was designed trained and tested using MATLAB. Impulse fault classification obtained with the RBF network for the test data and the complete dataset are shown in Fig.8 and Fig.9 respectively.

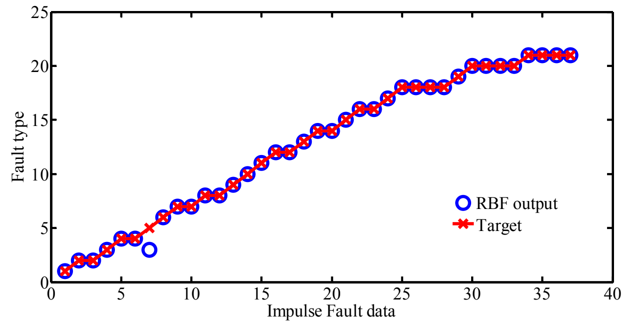

Fig.8. Impulse fault classification obtained with the RBF network for the test data

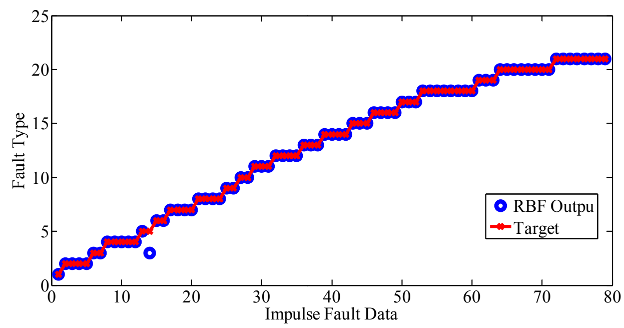

Fig.9. Impulse fault classification obtained with the RBF network with the entire dataset

Table 3. Defined fault types and assigned fault numbers

Fault types	*Fault No.*
NF	1
SF1/SF2/SF10/SHF9	2
SF3/SF9	3
SF4/SF5/SF6/SF7/SF8	4
SHF9SF7,SHF8	5
SHF9SF1&SHF9SF6	6
SHF9SF2-5	7
SHF7,SHF7SF8-10	8
SHF8SF6-7	9
SHF8SF1,SHF8SF5	10
SHF8SF2-4	11
SHF6,SHF6SF8-10	12
SHF7SF1-3	13
SHF5,SHF5SF8-10	14
SHF6SF1-3	15
SHF4SF8-10	16
SHF5SF1-3	17
SHF3,SHF3SF4-10	18
SHF4SF1-3	19
SHF2,SHF2SF4-10	20
SHF1,SHF1SF4-10	21

Hardware realization of Radial Basis Function Neural Network on spartan 6 fpga using xilinx system generator for dsp

The SIMULINK model for implementing the trained RBF neural network is developed using XILINX system generator blocks as given in Fig.10. The input data to the RBF network is fed from the ROMs storing the extracted Features. The subsystem representing the hidden RBF layer is implemented with adder and multiplier blocks to compute the Euclidean distance followed by an Mcode block to implement the radial basis function. Fig.11 shows the simulink model developed for the hidden RBF layer subsystem. The Output layer of the RBF Network is a linear layer whose weights are stored in a ROM and the bias for this layer is stored as a constant. Simulink model developed for implemtation of this layer is given in Fig.12. The response of the SIMULINK model of RBF network obtained in the connected scopes during simulation is given in Fig.13.

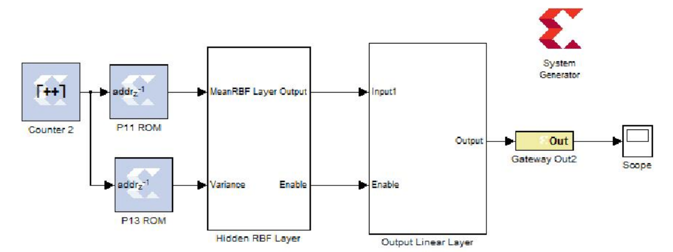

Fig.10. Simulink model of the RBF network constructed using Xilinx System generator toolbox

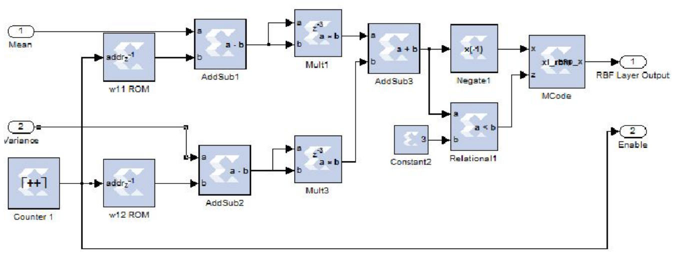

Fig.11. Simulink model for hidden RBF layer computation subsystem

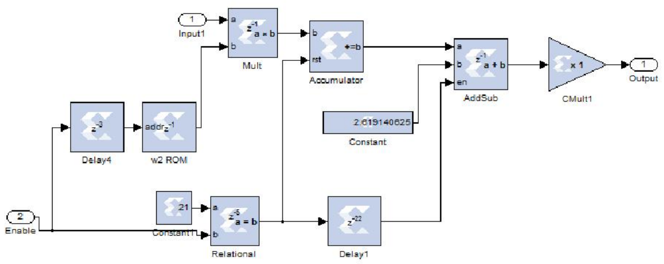

Fig.12. Simulink model for Output linear layer computation subsystem

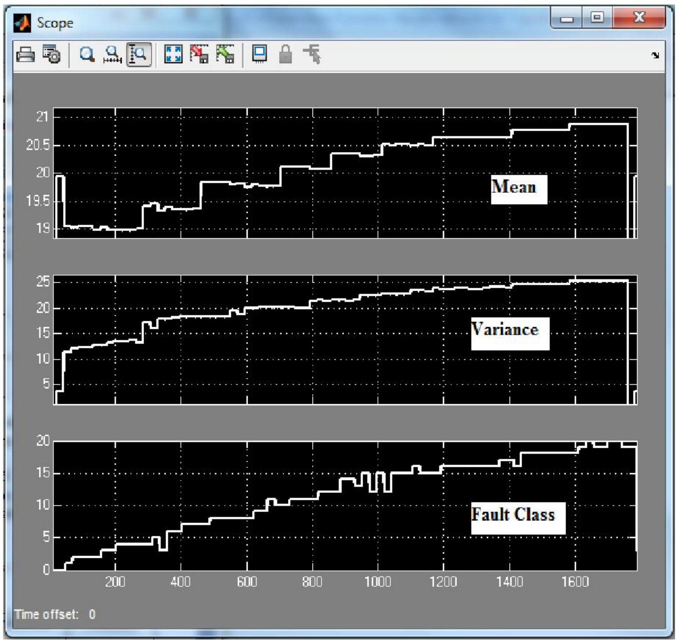

Fig.13. Scope waveforms of Mean, Variance and Fault Class obtained during simulation

The DWT Based feature extraction scheme designed and implemented by the author (Vanamadevi *et al.,* 2014) is combined with RBF NN to achieve the transformer Impulse fault classification scheme. The recorded winding current samples are stored in a ROM and is passed through DWT feature extraction scheme whose outputs namely mean and variance are fed as inputs to RBF network which finally detects the presence of fault and identifies the fault class.

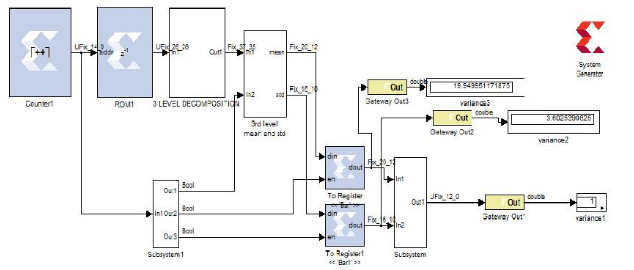

Fig.14. Simulink model of the RBF NN based Impulse fault classification scheme constructed using Xilinx System generator toolbox

The general purpose SPARTAN6 FPGA kit, which has XC6SLX25-3FTG256 IC developed by Xilinx Inc., is used for implementation as shown in Fig.15. Firstly the hardware realization of RBF network is carried out whose response recorded using DSO is given in Fig.16 and the device utilization summary is given in Table 4. The response of Impulse fault classification scheme comprising of DWT feature extraction scheme and RBF network for no fault winding current data is shown in the Fig.17. The response for simultaneous presence of series fault at section 10 and shunt fault at section 2 is given in Fig.18.

Fig.15. Experimental setup for downloading the design in SPARTAN6 FPGA

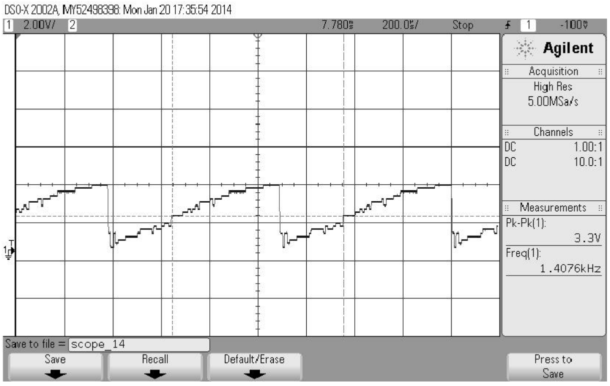

Fig.16. The response of the trained RBF network realized in SPARTAN6 FPGA recorded using DSO for the entire dataset

Table 4. Device utilization summary

Device Utilization Summary			
Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1,030	30,064	3%
Number of Slice LUTs	1,490	15,032	9%
Number used as logic	1,124	15,032	7%
Number used as Memory	217	3,664	5%
Number of occupied Slices	519	3,758	13%
Number of MUXCYs used	912	7,516	12%
Number of LUT Flip Flop pairs used	1,706		
Number of bonded IOBs	93	186	50%
Number of DSP48A1s	38	38	100%

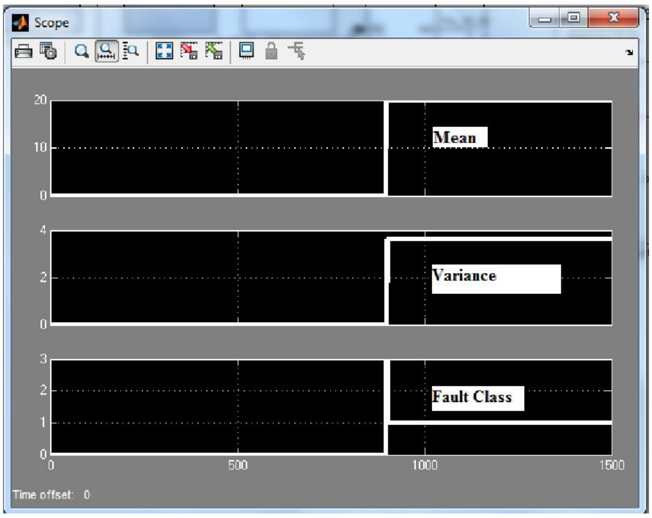

Fig.17. Scope waveforms of Mean, Variance and Fault Class obtained during simulation with no-fault current samples loaded in ROM

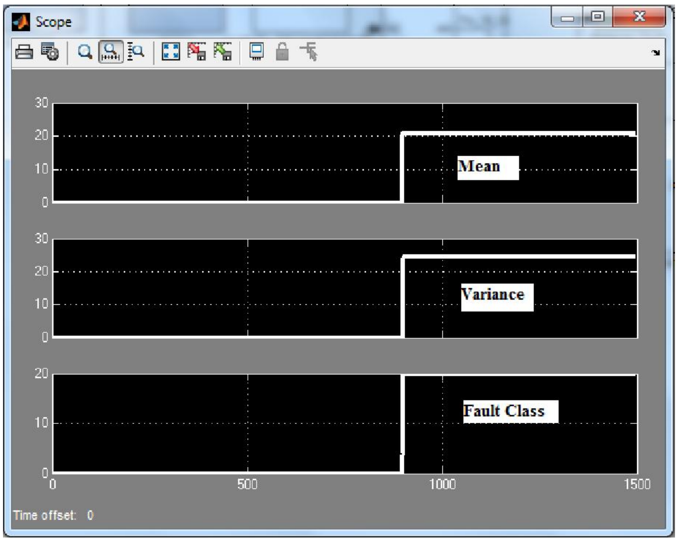

Fig.18. Scope waveforms of Mean, Variance and Fault Class obtained during simulation with simultaneous presence of series fault at section 10 and shunt fault at section 2 current samples loaded in ROM

Thus the RBF network is constructed with 21 hidden nodes whose radial basis functions having centers as the cluster centers of the 21 clusters and width parameter made equal to 1. The RBF network which is implemented using MATLAB coding had the classification accuracy of 97%. The classification accuracy has got reduced in the hardware realized RBF network as we reduced the word length of signals at various blocks since the scheme exceeded the capacity of SPARTAN6 FPGA and hence we are carrying out trials with modification in xilinx blocks usage.

Conclusion

FPGA components available today have usable sizes at an acceptable price. This makes them effective factors for cost savings and time-to-market when making individual configurations of standard products. A time consuming and expensive redesign of a board can often be avoided through application-specific integration of IP cores in the FPGA - an alternative for the future, especially for very specialized applications with only small or medium volumes. The proposed scheme with the DWT based feature extraction and the RBF network based impulse fault classification classified efficiently the finely defined fault types. This scheme has been found to classify successfully the simultaneous presence of multiple minor faults treated in this work.

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