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REVIEW ARTICLE

ANALYSIS AND SIMULATION OF POWER CONSUMPTION FOR SRAM

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ABSTRACT

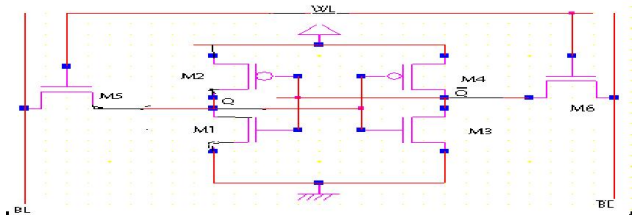
Static access memory (SRAM) is a building block of several logic circuits. SRAM is a fast memory which consumes low power. It is a fundamental building block of central processing unit of a computer. In this paper we design a low power circuit for 64 bit 5T SRAM using bottom-up approach. We use 0.12 micron meter technology and 90 neno meter technology for designing and simulation low power dissipation SRAM with dsch and micro wind. In this paper we simulate that reduction of power consumption in .12 micro technologies and 90 neno meter technology is 93% and 94% respectively.

INTRODUCTION

SRAM is the building block of several logic circuits. SRAM is a very fast and low power memory. It is essential to understanding how an SRAM is work and how it designs for building any advanced logic circuits. Using this knowledge and experience, we can design more complex integrated circuits. For designing the SRAM we will follow the principle "Computer Hardware" Which uses a modular design that consists of smaller, more manageable blocks, some of which can be re-used. We will first design one bit SRAM instead of designing the 64-bit SRAM then put 64 one bit SRAM together to make 64 bit SRAM. SRAM is the Static Random Access Memory in which the word static means the stored data can be retained indefinitely, without any need for a periodic refresh operation as long as a sufficient power supply voltage is provided.

Block diagram

A conventional SRAM uses six MOSFETs (2 PMOS and 4 NMOS) to store each memory bit. The memory bit-cell has two CMOS inverters connected back to back (M1, M3, and M2, M4) which is called storage cell. This storage cell has two stable states which are denoted as 0 and 1. Two more pass transistors (M5 and M6) are the access transistors controlled by the Word Line (WL), To access (read and write) the data contained in the memory cell there are two bit lines. Access (read/ write) from the cell is enabled by the word line (WL in figure) which controls the two *access* transistors M_5 and M_6 which control whether the cell should be connected to the bit lines: BL and $\overline{BL}$, which are used to transfer data for both read and write operations. An SRAM cell has three different states it can be in: *standby* where the circuit is idle, *reading* when the data has been requested and *writing* when updating the contents. The three different states work as follows:



Standby

If the word line is not activated (WL=O), the *access* transistors M_5 and M_6 disconnect the storage cell from the bit lines. The two cross coupled inverters formed by $M_1 - M_4$ will continue communicate to each other as long as they are connected to the supply.

Reading

Assume at Q the content of the memory is a 1,Starting of read cycle is done by precharging both the bit lines to a logical 1, then activate the word line WL, enabling both the *access* transistors (M_5 and M_6). The second step occurs when the

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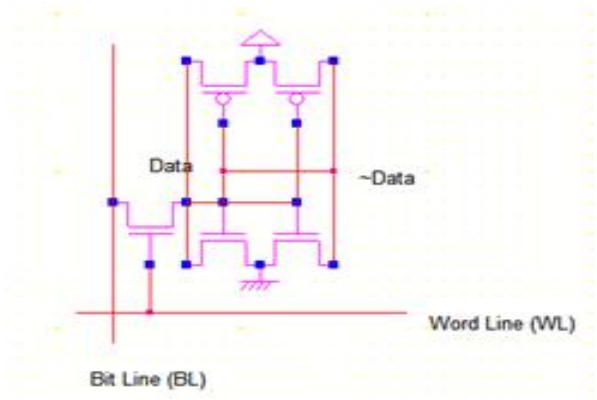
values stored in Q and $\overline{Q}$ are transferred to the bit lines which leaving BL at its precharged value and discharging $\overline{BL}$ through M_1 and M_5 to a logical 0. On the BL side, the transistors M_4 and M_6 pull the bit line toward V_{DD}, a logical 1. If the content of the memory is a 0, the opposite process happens in which $\overline{BL}$ would be pulled toward 1 and BL toward 0.

Writing

The write cycle begins by applying the value to be written to the bit lines. If we want to write a 0, we would apply a 0 to the bit line, i.e. setting $\overline{BL}$ to 1 and BL to 0. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then active and the value that is to be stored is latched in.

Proposed work (5T SRAM)

The proposed simulation steps consist in writing a 0 →1, and then reading the 1. In a second phase, we write a 1→ 0, and read the 0. The Bit Line signal is controlled by pulses. If the word line is not asserted, the *access* transistor disconnects the cell from the bit line. The two cross coupled inverters formed by will continue to support each other as long as they are connected to the supply. Assume that the content of the memory is a **1**, stored at Q. The read cycle is started by precharging the bit line to a logical **1**, then asserting the word line WL, enabling the access transistor. The second step occurs when the values stored in Q and $\overline{Q}$ are transferred to the bit line by leaving BL at its pre charged value. If the content of the memory were a **0**, the opposite would happen .The start of a write cycle begins by applying the value to be written to the bit line. If we wish to write a **0**, we would apply a **0** to the bit line, i.e. BL to **0**.

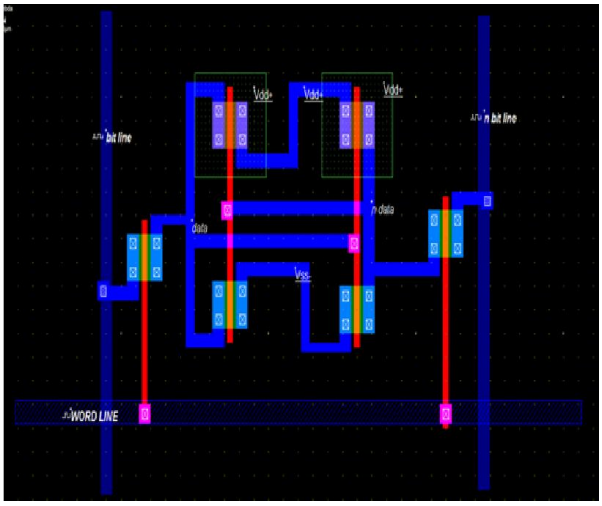


64-BIT SRAM

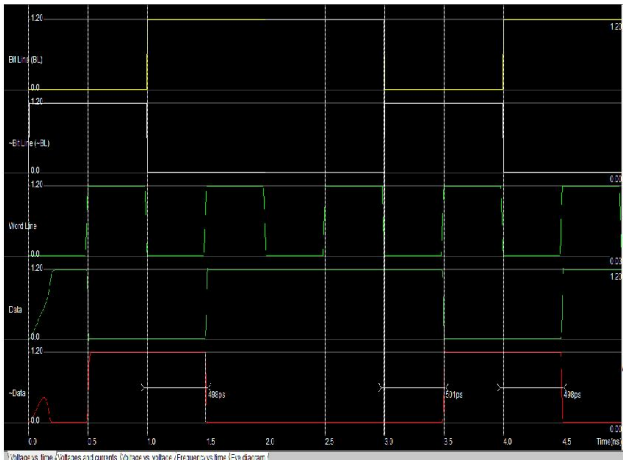
In this section given detailed simulation analysis of the 64-bit SRAM cell. We estimate the impact of the SRAM cell on the power dissipation. The schematic of SRAM cell is designed and implemented by using Micro wind 3.1. The design has been simulated using CMOS. 12µm and 90nm technology. Then we design a 64-bits memory by using 5T SRAM cell and the result is compared with Conventional 6-T SRAM cell. The transistors reduce dynamic power consumption during write operation through proper charging and discharging of the bit lines. In the conventional 6T SRAM cell, one of the two bit lines must be discharged to low regardless of written value, therefore the power dissipation in both write "0" and "1" is more. In our 5T SRAM cell as shown in figure, we are preventing any single bit line from being discharged during write "0" as well as write "1" mode Read/write memory circuits are designed to permit the modification (writing) of data bits to be stored in the memory array, as well as their retrieval (reading) on demand. The data storage cell, i.e. one bit memory cell in SRAM arrays invariably consists of a simple latched circuit with two stable operating points (states), which depend on the preserved states of the two inverter latch circuit. The data being holding in the memory cell will be represented either as logic ' 0 ' or logic ' 1 '. The data contained in the memory cell access (R/W) via the bit line. We need at least one switch, which is controlled by the corresponding word line. i.e. the row address selection signal shown in the figure .Usually to complementary access switches consisting of NMOS pass transistor are implemented to connect the 1-bit SRAM cell to the complementary bit lines (columns). The access transistors are turned on whenever a word line (row) is activated for read and write operation, connecting the cell to the complementary bit line columns. A CMOS memory cell thus draws current from the power supply only during a switching transition. The low standby power consumption has certainly been a driving force the increasing prominence of high density CMOS SRAMs. Cell 1 will work when BL1 is activated; in that time WL1 is activated. Cell 2 will work when BL2 is activated; in that time WL1 is activated. Cell 3 will work when BL3 is activated; in that time WL1 is activated and so on. Cell 8 will work when BL1 is activated; in that time WL2 is activated. Cell 9 will work when BL2 is activated; in that time WL2 is activated and so on

RESULTS

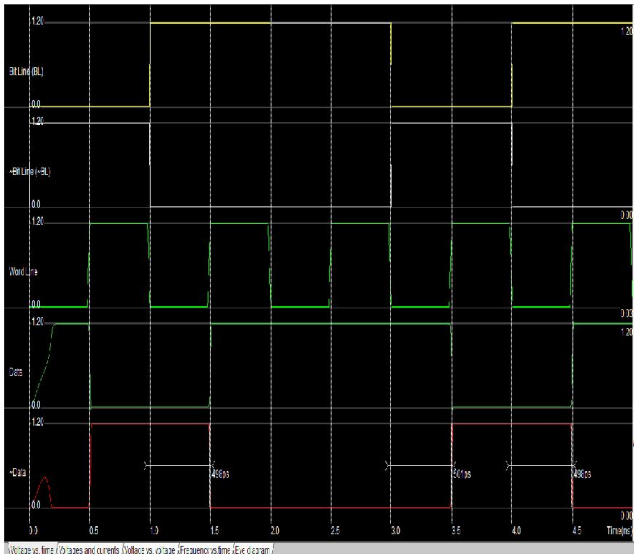
1. Layout design of 1-BIT SRAM (6T)



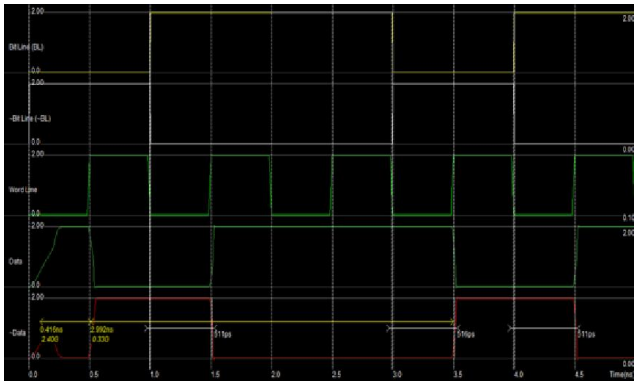
2. Simulation of 1-BIT SRAM (6T)



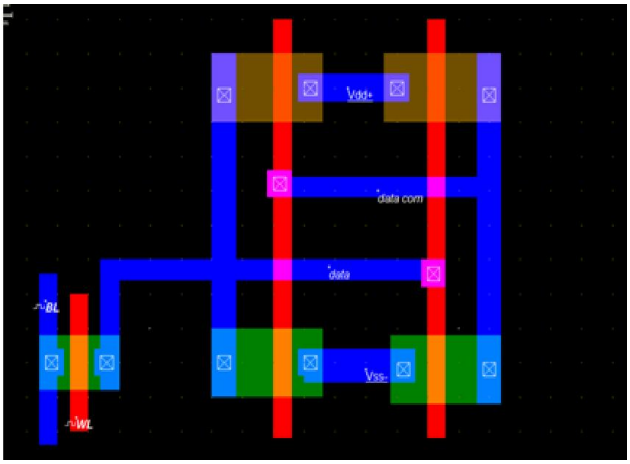
3. Simulation of 64-BIT SRAM by using .12µm Technology voltage vs time SRAM



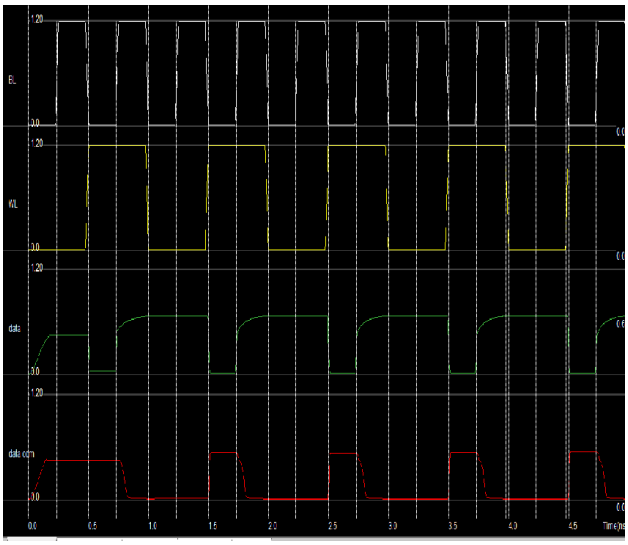
4. Simulation of 64-BIT SRAM by using 90nm Technology Voltage Vs Time wave form



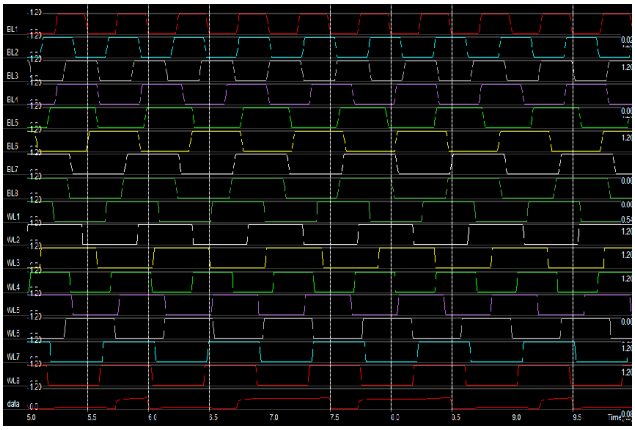
5. Layout design of 1-BIT SRAM (5T)



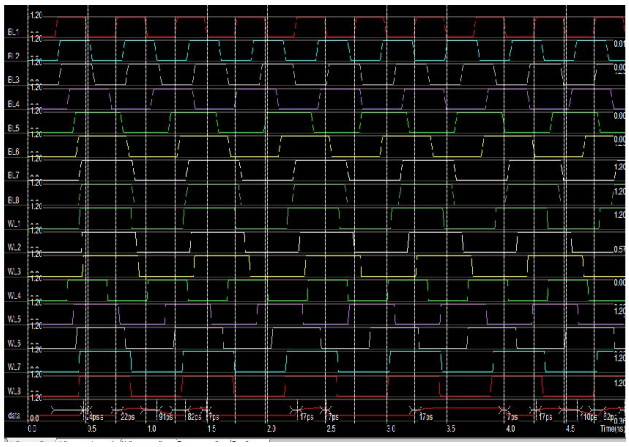
6. Simulation of 1-BIT SRAM (5T)



7. Simulation of 64-BIT SRAM gate by using 0.12µm technology



8. Simulation of 64-BIT SRAM gate by using 90nm technology



Conclusion and future scope

This section includes conclusion drawn on basis of functional simulation results as well as implementation of SRAM. By using 0.12 micron and 90nmtechnology we design5T SRAM and we can perform read and write operation. It is a fundamental building block of the central processing unit of a computer. RAM is a building block of several circuits. The 64 bit SRAM unit has been designed with MICROWIND and DSCH2. The MICROWIND program allows the designer to design and simulate an integrated circuit at physical description level. DSCH2 allow design circuit of digital logic. To implement 64 bits 5T SRAM to 6T SRAM, 5T SRAM reduce 93% of power dissipation in .12 μm and 94% in 90 nm technologies. Now to implement a 64bits 5T by using a 0.12μm gives the advantage of reduction of power dissipation in 45% and reduction of delay in 51% and reduction of area is 30% with comparison to 90nm technology. The physical (mask layout) design of CMOS logic gates is an iterative process which starts with the circuit topology (to realize the desired logic function) and the initial sizing of the transistors (to realize the desired performance specifications). Future work could be extended to optimizing unit capacitance SRAM. Knowing the fabrication run being used and error percentage in process would give us feedback for designing with smaller capacitors. Realizing logic designs with smaller capacitors will reduce the power dissipation and make the layout more area efficient.

Further work could also include extending the current design to include more number of input bits for the SRAM. In future Dual-SRAMs are used to execute instructions concurrently for fine-grained parallelism.

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