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RESEARCH ARTICLE

A REVIEW PAPER ON TECHNIQUES OF LEAKAGE REDUCTION IN VLSI CIRCUITS

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ABSTRACT

The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast speed Typically, the required computational and information processing power of these applications is the driving force for the fast development. We propose a technique called self controllable voltage level (SVL) technique which significantly reduces the leakage current. Dynamic power dissipation is also reduced. In the proposed technique, we reduce 93% of leakage current by using self controllable voltage level technique and This technique is applied in 1- bit adder and simulation is done by using a MICROWIND 3.1 and DSCH 2 with 90nm technology.

INTRODUCTION

In this project several leakage reduction technique is studied and analysed, after which a particular leakage reduction technique is selected. Selected technique is self controllable voltage level technique. This technique is further improved to enhance the system of cmos vlsi circuit. A full adder is the required cmos circuit whose leakage current reduction is determined with the help of svl technique. Heng-Yao Lin, Chi-Sheng Lin, Lih-Yih Chiou, and Bin-Da Liu *et al*. (2004) has develop logic gate design with low leakage. Traditionally, the subthreshold leakage through a logic gate depends on the applied input vector. They have used stacking of an extra transistor in large leakage path to reduce leakage power. The proposed structure induces low leakage current under all possible inputs. Compared to the conventional CMOS logic circuit design, the simulation results shows that the proposed logic circuits not only reduce significant leakage power dissipation, but also keep similar circuit performance as conventional CMOS logic circuits. They have studied different leakage reduction techniques. Different leakage reduction techniques are pn junction Reverse Bias Current, Subthreshold Leakage, Leakage Reduction Using Transistor Stacks. The transistor stacking technique is proven to be very effective in reducing subthreshold leakage in standby-mode. In this paper, a novel frame of logic gate by transistor stacking is proposed and effective reduction of overall leakage in a stack of transistors and in simple logic gates is analysed. The proposed low leakage logic circuit was simulated with the TSMC 0.18 μm one poly six metal CMOS process. The simulation results shows that the proposed circuit reduces the maximum leakage power in conventional logic circuit under acceptable speed performance. Based on the proposed circuits, the circuit design has the feature of low leakage current without caring about its input vector. Mutoh *et al.* (1995), designed the 1-V power supply high-speed digital circuit technology with multi-threshold voltage CMOS which presents the analysis for leakage current and propagation delay in CMOS circuits by implementing LECTOR and MTCMOS techniques using nanoscale technologies. Effective stacking of transistors in the path from supply voltage to ground is used in the Leakage Control Transistor (LECTOR) technique. The main concept behind this technique is that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." Md. Asif Jahangir Chowdhury, Md. Shahriar Rizwan and M.S.Islam *et al*. (2012) have tried to reduce static power of a VLSI Design using Variable body biasing. They show in cmos integrated circuits static power consumption is becoming more dominant due to increase in power density. They shows how to reduce static power consumption by different methods. In this paper they introduced variable body biasing technique to reduce static power consumption in cmos vlsi design. They took under consideration the main factor like area and circuit performance. Previous circuit level approaches are being studied for subthreshold leakage power reduction. Some of them are as follows Sleep transistor approach, Sleepy Stack approach, Sleepy Keeper approach, Dual sleep approach, Dual stack approach. In the end Variable body biasing approach is

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finalized to reduce static power consumption Here we have to implement the 1-bit full adder by using a self controllable voltage level technique in which circuit is divided in two parts upper SVL and lower SVL. For controlling the leakage current pre charge circuit is added. Power consumption has become the limiting factor functionality that can be placed in the electronic devices. The full circuit depiction is obtained from the initial layout. Then the improved design will be implemented into a new layout and the design-analysis cycle will be repeated until all of the design specifications are met. Each such combined structure can be realized in CMOS as follows, the AND terms are implemented by series-connected NMOS transistors, and the OR terms are implemented by parallel-connected NMOS transistors. Thus, the NMOS net may consist of nested series-parallel connections of NMOS transistors between the output node and the ground .For translating the gate-level design into a transistor-level circuit description. The sum out and the carryout functions are represented by nested AND-OR- NOR structures. The input variables are applied to the gates of the NMOS and complementary PMOS transistors.. The resulting transistor-level design of the CMOS 1-bit adder circuit. The circuit contains a total of 14 NMOS and 14 PMOS transistors, together with the two CMOS inverters which are used to generate the outputs and 4 extra transistors is added in the circuit for reducing the leakage current. The transistor sizes means of channel width size depends on the number of transistors. Initially, we will design all NMOS and PMOS transistors with a (W/L) ratio which is the minimum transistor size. The initial layout using minimum-size transistors is the 1-bit adder circuit is generated. Increasing the transistor (W/L) ratios also increases the gate, source, and drains areas and as a result, increases the parasitic capacitances loading the logic gates. Hence, the resizing of transistors is definitely an iterative process which involves several cycles of successive layout modification, circuit extraction, and simulation. We will design all NMOS and PMOS transistors with a (W/L) ratio which is the minimum transistor size.

Leakage Reduction Technique

- Forced P-MOS Transistor Inverter
- Forced N-MOS Transistor Inverter
- Sleep Transistor Approach
- Sleepy Stack Approach
- Sleepy Keeper Approach
- Stack Approach
- Dual Sleep Approach
- Dual Stack Approach
- LECTOR technique
- Self Controllable Voltage Level Technique.

We have studied number of technique for leakage reduction. We have selected a Self Controllable Voltage Level Technique.

Proposed Work

The transistor-level design of the CMOS 1- Bit adder circuit is shown in Figure 1. The circuit contains a total of 14 NMOS and 14 PMOS transistors, together with the two CMOS inverters which are used to generate the outputs. Here basically three input A, B, C and two output sum and carry out. The Boolean expression of these two are

$$SUM = A\,B\,C + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,\overline{C}\,B$$

$$= A \oplus B \oplus C \quad (1)$$

$$carry\_out = AB + AC + BC \quad (2)$$

Where
A, B, C, = three inputs of adder
Sum = sum output of adder
Carry_out = carry output of adder

In equation (1) shows the sum output and equation (2) shows the carry output [Sung-Mo kang yusef leblebici 2003]. This equation is implemented by using a CMOS technology in which NMOS is solved by without compliment and PMOS is implemented by with NMOS. Connection is done like an if add sign then shown then parallel combination occurs and if dot sign shown then series combination occurs. The layout of the full-adder circuit shown in Figure 2 in which have been designed using the simple layout optimization strategy. However, that all NMOS and PMOS transistors in this layout have the same (W/L) ratio. In Figure 7 shows the voltage vs current waveform in which the leakage current is about 0.334ma.

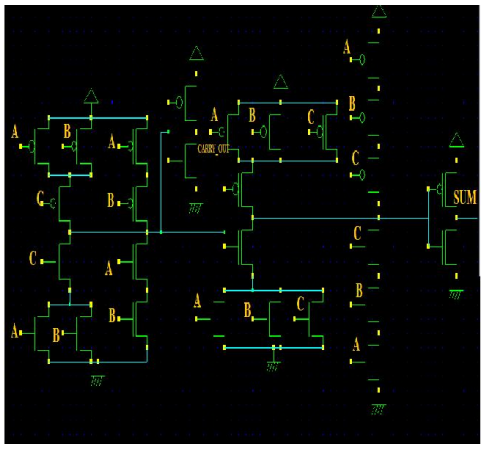

Figure 1. Transistor-level schematic of the one-bit full-adder circuit

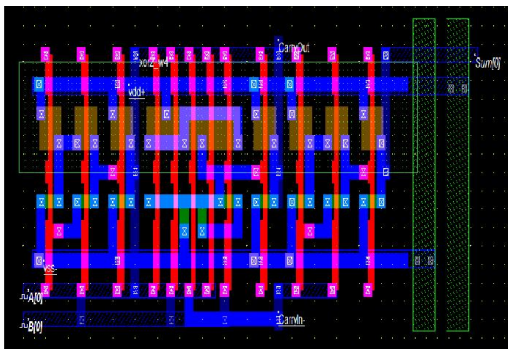

Figure 2. Layout diagram of 1-bit adder

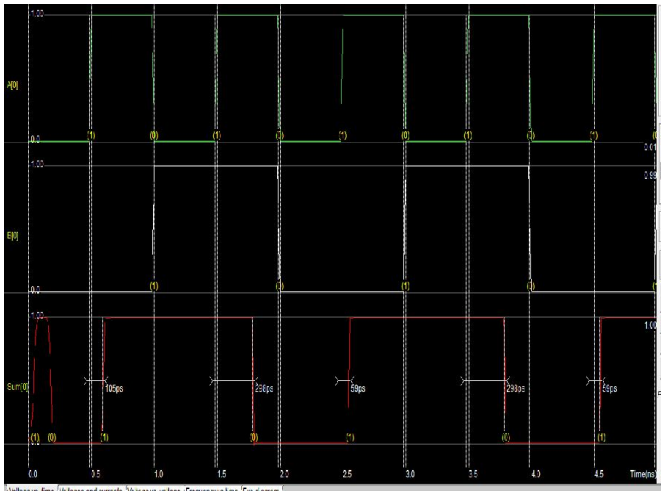

Figure 3. Waveform of voltage vs. time

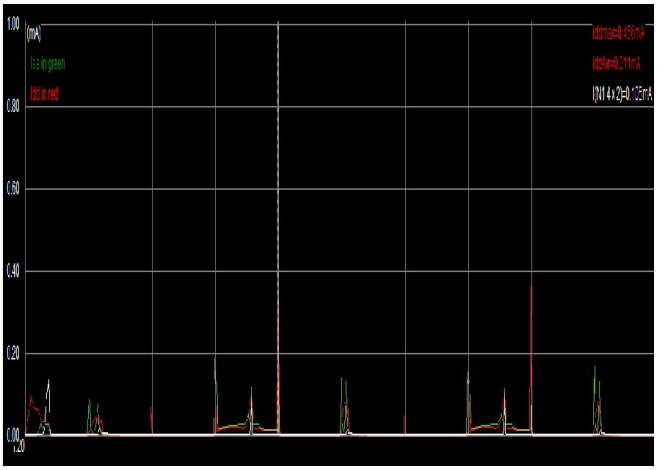

Figure 4. Waveform of voltage vs. current

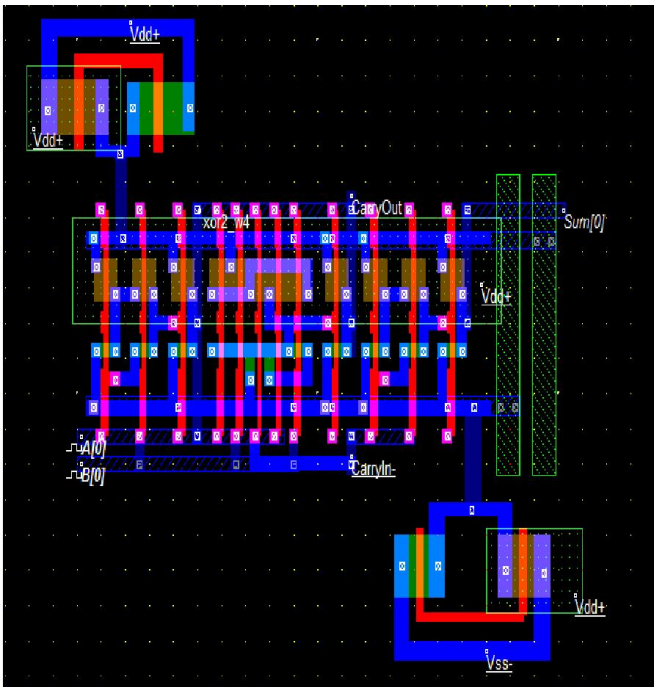

Figure 5. Layout diagram of 1-bit adder with SVL Technique

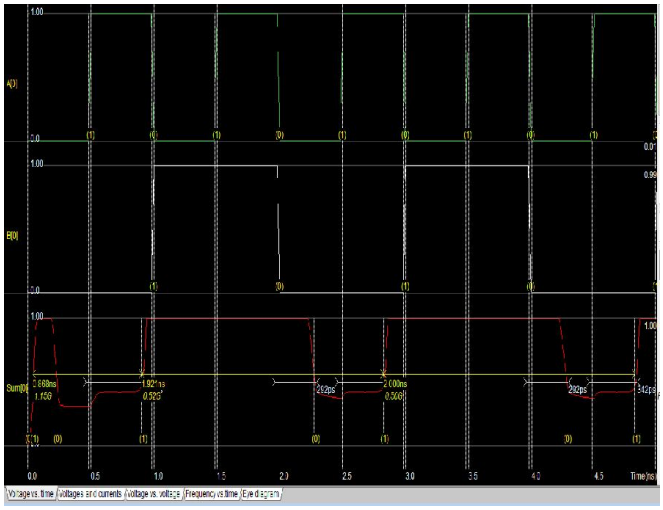

Figure 6. Waveform of voltage vs. time with SVL Technique

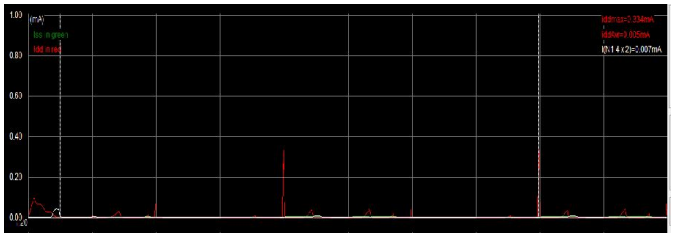

Figure 7. Waveform of voltage vs. currents with SVL Technique

Circuit Simulation Result

The simulation of the one-bit CMOS full adder is implemented in MICROWIND3.1. and DSCH 2 The 1-bit adder in which accepts 3 -bit binary numbers as input and produces the binary sum at the output and carry output. Within the MICROWIND 3.1 used a 90nm technology. The waveform of voltage versus time shown in Figure 3 in which carry is high only when the two or three high signal is added otherwise it is low and sum is high if any of three signals is high at a time. In figure 4 shows the voltage versus current waveform in which the leakage current is about 0.456ma. In figure 5 shows the layout diagram of 1-bit adder with self controllable voltage level (SVL) Technique in which used an upper SVL and lower SVL for controlling the leakage current. There are layout design of 4-bit adder implemented with the use of self controllable voltage level technique of four transistors.

Table 1. Parameter of 1 bit adder

Process technology	90nm
Power supply voltage	1v
Pre charge voltage	1v

Table 2. Simulation result of svl based 1 bit adder in term of leakage current

Circuit	Leakage current
1 Bit Adder without SVL	0.456ma
1 Bit Adder with SVL	0.334ma

Conclusion

The two main task are presented here one is leakage current reduction and another is dynamic power reduction. so reducing these two factors the speed increase in the full adder circuit. 1-bit adder is simulated by using microwind3.1 and dsch2 software with 90nm technology. here leakage current reduction (svl) technique is used in 1- bit adder. by using a self controllable voltage technique to reduce the 93% of leakage current in 1-bit adder.

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